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APPLICATION NO.	FI	LING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO	
09/851,433 05/09/2001		Jun Koyama	0756-2307	2113		
31780	7590	08/10/2004		EXAMINER		
ERIC ROBINSON PMB 955				KOVALICK, VINCENT E		
21010 SOUTHBANK ST.				ART UNIT	PAPER NUMBER	
POTOMAC FALLS, VA 20165			2673	111		
			DATE MAILED: 08/10/2004			

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)			
•	,		KOYAMA ET AL.			
Office Action Summary		09/851,433 Examiner	Art Unit			
	• • • • • • • • • • • • • • • • • • •					
	The MAILING DATE of this communication app	Vincent E Kovalick	correspondence address			
Period fo	· · · · · · · · · · · · · · · · · · ·					
THE - External after - If the - If NO - Failth	MAILING DATE OF THIS COMMUNICATION. Insions of time may be available under the provisions of 37 CFR 1.1 In SIX (6) MONTHS from the mailing date of this communication. In period for reply specified above is less than thirty (30) days, a replector of the reply is specified above, the maximum statutory period of the provision o	36(a). In no event, however, may a reply be t y within the statutory minimum of thirty (30) da will apply and will expire SIX (6) MONTHS from e, cause the application to become ABANDON	ays will be considered timely. In the mailing date of this communication. IED (35 U.S.C. § 133).			
Status						
1) 又	Responsive to communication(s) filed on 04 Ju	une 2004.				
-		action is non-final.				
3)□	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.					
Disposit	ion of Claims					
5)⊠ 6)⊠ 7)□	Claim(s) 33-44 and 55-60 is/are pending in the 4a) Of the above claim(s) is/are withdraw Claim(s) 33-44,59 and 60 is/are allowed. Claim(s) 55-58 is/are rejected. Claim(s) is/are objected to. Claim(s) are subject to restriction and/or	wn from consideration.				
Applicat	ion Papers					
	The specification is objected to by the Examine					
10)	The drawing(s) filed on is/are: a) acc					
	Applicant may not request that any objection to the					
11)	Replacement drawing sheet(s) including the correct The oath or declaration is objected to by the Ex					
Priority (under 35 U.S.C. § 119					
12)⊠ a)	Acknowledgment is made of a claim for foreign All b) Some * c) None of: 1. Certified copies of the priority document 2. Certified copies of the priority document 3. Copies of the certified copies of the priority document application from the International Bureau See the attached detailed Office action for a list	s have been received. s have been received in Applicative documents have been received in Rule 17.2(a)).	tion No ved in this National Stage			
Attachmer		_				
	ce of References Cited (PTO-892) ce of Draftsperson's Patent Drawing Review (PTO-948)	4) Interview Summar				
3) 🔲 Infor	ce of Draftsperson's Patent Drawing Review (PTO-948) mation Disclosure Statement(s) (PTO-1449 or PTO/SB/08) er No(s)/Mail Date	Paper No(s)/Mail E 5) Notice of Informal 6) Other:	Patent Application (PTO-152)			

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DETAILED ACTION

Response to Amendment

1. This Office Action is in response to Applicant's Amendment dated June 4, 2004 in response to USPTO Office Action dated January 2, 2004. The cancellation of claims 1-32 and 45-54, the amendments to claims 35, 37-39 and 44, the addition of new claims 55-60 and Applicant's Remarks have been reviewed and entered in the record.

Regarding Applicant's Remarks, the cancellation of rejected claims 28 and 29 and the amendments to claims 37-39 and 43-44 renders the rejection of said claims moot, said claims are now reconsidered in light of the amendments to claims 37-39 and 43-44 as indicated hereinbelow.

Claim Rejections - 35 USC § 103

- 2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 3. Claims 55-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato et al. (USP 5,841,497).

Relative to claims 55 and 57, Sato **teaches** a Liquid Crystal Device (LCD) and Liquid Crystal Apparatus (col. 3, lines 9-67 and col. 2, lines 1-5); Sato et al. further **teaches** a device comprising a pixel portion over a substrate; a data line side driver circuit provide over the substrate and operationally connected to the pixel portion; a memory portion provided over the

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substrate and operationally connected to the data line side driver circuit; a memory control circuit provided over the substrate and operationally connected to the memory portion; or a memory portion and the data line side driver circuit, wherein an image signal is transferred in a direction from said memory control circuit, said memory portion and said data line side drive circuit (col. 65, lines 16-24 and Fig. 2). Still further, Sato et al. teaches a liquid crystal device (LCD) matrix (pixels) structured on a substrate (col. 4, lines 29-34).

The difference between the teaching of Sato et al. and that of the instant invention is that Sato et al. does not specifically teach casting the pixel matrix and the associated memory and control elements on the same substrate.

Though Sato et al. teaches an LCD structured on a substrate, Sato et al. **does not**teach the data line side driver circuit, memory and memory control circuit provided over the substrate with the pixel. matrix; said physical layout being in common practice and well known in the art.

Because the said practice of providing the display elements (pixels) and the supporting memory and control circuitry co-resident on the same substrate is well know and in common practice in the art, it would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Sato et al. the feature of casting the pixel matrix and the associated memory and control logic on the same substrate in order to provide an arrangement that would optimize processing speed and minimize the structural elements that makeup the display unit.

It would have been obvious to a person or ordinary skill in the art at the time of the invention

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that the features as taught by Sato et al. satisfy the limitations taught in claims 55 and 57 of the instant invention.

Regarding claims 56 and 58 Sato et al. further **teaches** the device memory being a (VRAM) selected from the family of Random Access Memory devices (col. 65, lines 25-33).

Allowable Subject Matter

- 4. Claims 33-44 and 59-60 are allowed.
- 5. The following is an examiner's statement of reasons for allowance:

Regarding claim 33, the major differences between the teachings of the prior are of record (USP 6,646,288, Yamazaki et al.; USP 6,323,836, Shin and USP 5,841,497, Sato et al.) and that of the instant invention is that said prior art of record **does not teach** a semiconductor device comprising at least a pixel portion, a data line side driver circuit, a scanning line side driver circuit and a memory portion wherein the pixel portion is formed over a first substrate, the data line side driver circuit and said memory portion are formed over a second substrate and said scanning line side drive circuit is integrally formed over a third substrate.

Relative to claim 59, major differences between the teachings of the said prior are of record and that of the instant invention is that said prior art of record **does not teach** a device comprising an input terminal; a first control circuit operationally connected to the input terminal; a second control circuit operationally connected to the first control circuit; at least one first memory operationally connected to the first control circuit; a memory control circuit operationally connected to the second control circuit; a memory portion operationally connected

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to the memory control circuit; a data line side driver circuit operationally connected to the memory portion; and a pixel portion operationally connected to the data line side driver circuit, wherein all of the first control circuit, the second control circuit, the first memory, the memory control circuit, the memory portion, the data line side driver circuit and the pixel portion are provided adjacent to a same substrate.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U. S. Patent No.	6,118,502	Yamazaki et al.
U. S. Patent Application No.	2003/0160236	Yamazaki et al.
U. S. Patent Application No.	2003/9958195	Adachi et al.

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

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however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Responses

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent E Kovalick whose telephone number is 703 306-3020. The examiner can normally be reached on Monday-Thursday 7:30- 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703 305-4938. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vincent E. Kovalick

August 4, 2004

BIPÍN SHALWALA SUPERVISORY PATENT EXAMINER

TECHNOLOGY CENTER 2600